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13. ABSTRACT *(Maximum 200 Words)*

1) The first semiconductor thermionic cooler was demonstrated during the past year. It was implemented in InGaAsP and performs as predicted theoretically. The goal is demonstrating high cooling powers with materials that can be integrated with photonic devices i.e. InGaAsP. This should allow cost effective cooling of individual elements in wavelength devision multiplexing (WDM) components.

2) The first superlattice thermionic cooler was demonstrated. With the proper design of superlattices, we should be able to increase the thermal resistance without increasing the electrical resistance. This is needed in any thermionic or thermoelectric cooler; however, for virtually all semiconductors, higher thermal resistance and higher electrical resistance move together. This is important for getting larger temperature differences between hot and cold junctions.

3) The first p type thermionic cooler was demonstrated, although with poorer performance than predicted because of a contact resistance problem. Both p and n type thermionic cooler are needed to build integrated structures.

4) The theory of thermionic coolers was expanded to include Monte Carlo calculations of electron transport and model the coolers more accurately. The predicted results are slightly better than our earlier calculations based on a Richardson model, because ballistic transport of electrons results in energy being deposited preferentially closer to the hot junction.

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Final Report for

Heterostructure Integrated Thermionic Coolers

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Abstract

The first semiconductor thermionic cooler was demonstrated during the proposal period. It was implemented in InP. The goal is demonstrating high cooling powers with materials that can be integrated with photonic devices. This should allow cost effective cooling of individual elements in wavelength devision multiplexing (WDM) components. Both MOCVD grown InGaAs/InGaAsP and MBE grown InGaAs/InAlAs superlattices have been fabricated and characterized. With the proper design of superlattices, we should be able to further increase the thermal resistance without increasing the electrical resistance. This is needed in any thermionic or thermoelectric cooler; however, for virtually all semiconductors, higher thermal resistance and higher electrical resistance move together. This is important for getting larger temperature differences between hot and cold junctions. Cooling for both p and n type thermionic cooler are also demonstrated. This paves the road to build integrated structures with larger cooling areas. We have also performed BEEM measurements of carrier transport in single barrier GaAs/AlGaAs structures. The experimental results show that lateral momentum is not conserved in thermionic emission over metal-semiconductor interfaces. This can be used in the optimization of thermionic coolers. On the theoretical side, Monte Carlo calculations of electron transport in heterostructure coolers were performed. In order to optimize the cooler performance, we did extensive 2D and 3D simulations; we realized the importance of packaging in the overall cooling results. Significant improvements have been achieved with new packages. The best results for InP thin film coolers are ~1C cooling at room temperature and 2.2C cooling at 70C. This cooling over 1 micron thick barrier corresponds to cooling power densities on the order of 100W/cm^2. Theoretical predictions show that by reducing non-ideal effects one should be able to achieve 10-15C single-stage cooling with III-V based thermionic coolers. This is on the same order than the SiGe coolers developed under a different program (DARPA funded Heretic/Impact project). We were able to achieve 4.5C cooling at room temperature and 14C cooling at 250C with SiGe/Si superlattice structures.

Ballistic Electron Emission Spectroscopy

Bandedge discontinuities at the cathode and anode side of the device are crucial for selective emission of hot electrons and the performance of HIT coolers. A detailed analysis of the bandedges and the electron transport in the barrier layer was performed in Prof. Narayanamurti's group using a variable temperature Ballistic Electron Emission Microscope (BEEM) for analysis. An STM tip (at voltage V) is used to inject electrons into a metal film evaporated on the surface of the semiconductor. A third terminal is used to collect the transmitted current (I_C). By placing heterostructures within a Ballistic mean free path one can measure the characteristics of heterostructures such as these by measuring I_C as a function of heterojunction band offset. In addition, by scanning the tip one can get a spatial map of the transport.

In previous studies, we found that the BEEM current threshold for Au/GaAs/AlGaAs heterostructure system follows the composition dependence of the Γ valley in the direct bandgap regime of $0 \le x \le 0.45$. However, the absolute contributions of the conduction valleys were found to contradict to the assumption of transverse momentum conservation at the metal-semiconductor (m-s) interface. To consider electron scattering at the m-s interface, Smith, Narayanamurti et al. proposed the metal-semiconductor interface-induced scattering (MSIS) model. In the strong scattering limit, this model was found to describe the absolute magnitude of the experimentally observed BEEM current for Au/GaAs and Au/Si systems (see Fig. 1)

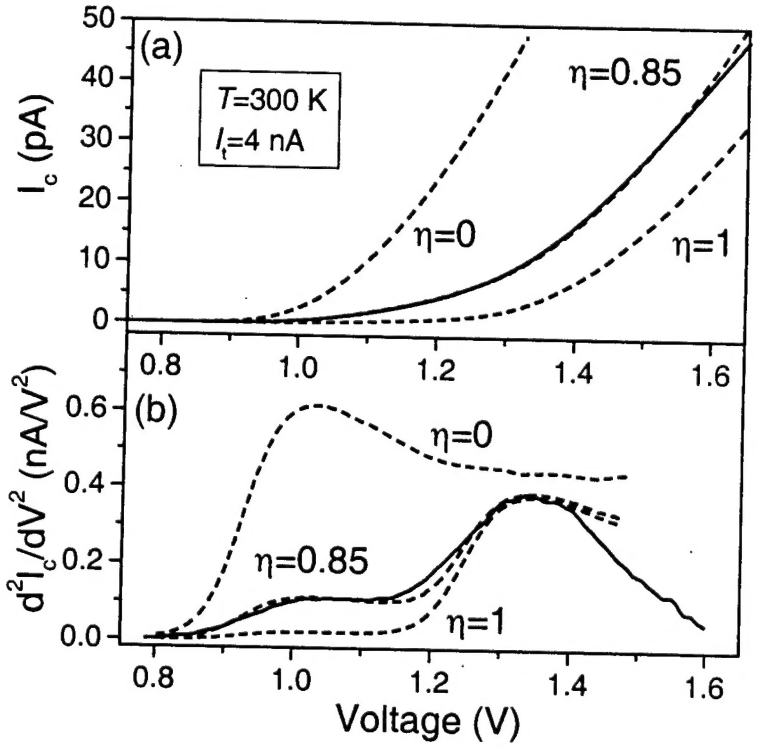


Fig.1 The room-temperature BEEM (a) and second dereivative-BEEM (b) spectra of Au/GaAs sample. The MSIS model calculations (dashed lines) are also presented for three values of η, the electron scattering probability at the metal-semiconductor interface.

Monte Carlo Simulation

The overall cooling capacity of a single barrier HIT cooler, with cathode side barrier height of ϕ_C, barrier thickness d and its thermal conductivity β, can be expressed as

$$Q_{TI} = \left[\Phi_C + 2\frac{k_B T_C}{e}\right]\cdot I - IV\left[\left(\frac{1}{2} - \frac{\lambda_E}{d}\right) - \frac{\lambda_E^2}{d^2}\left(e^{-d/\lambda_E} - 1\right)\right] - \frac{\beta}{d}\Delta T$$

where k_B is the Boltzmann constant, e the electric charge, T_C the cold side (cathode) temperature, and $\Delta T = T_H - T_C$. λ_E is the energy relaxation length for carriers. The dependence on electrical conductivity of the barrier (carrier mobility) is hidden in the I(V) relationship. This energy balance equation has three terms that describe thermionic cooling at the cathode, "Joule" heating in the barrier and heat conduction from the hot to the cold side. Thermionic cooling is equal to average energy of emitted electrons time the current. Assuming Boltzmann distribution for carriers, which is valid for barrier heights > $2k_BT$, this average energy is $(\phi_C + 2k_BT_C/e)$. The Joule heating term is IV times a coefficient, which takes into account the finite electronic energy relaxation length λ_E. In the limit of very thick devices, this coefficient reduces to 1/2 which is the result for pure diffusive transport. In the other limit of very short devices, the Joule heating term vanishes. In this case of ballistic transport, all of the electron's energy is deposited at the anode side.

In order to optimize HIT cooling devices, it is important to minimize Joule heating in the barrier. It is thus necessary to understand what are the main mechanisms that determine electronic energy relaxation length (λ_E) in semiconductors. For this purpose we will use Monte Carlo simulations of electron transport in GaAs. Other III-V semiconductors such as InP have similar characteristics. Ternary and quartenary compounds have in addition alloy scattering, but this is not expected to change energy relaxation considerably.

Fig. 2 displays the Joule heating as a function of distance for 5000 electrons injected over a 0.1 eV barrier into a 3 μm thick GaAs layer under an electric field of 5 kV/cm. It can be seen that, it will take about 1 μm before electrons reach equilibrium and lose energy equal to what they gain at steady state from the external electric field. Fig. 2 displays also the contribution of major scattering processes to electron energy relaxation as a function of distance. It can be seen that major scattering events responsible for energy relaxation at short distances (< 0.5μm) are polar optical phonon emission and absorption in the Gamma valley. At longer distances, there is a substantial population in the L valley. In this case, L-valley polar optical phonon emission and absorption and inter L-valley scatterings will start to contribute to the electronic energy loss mechanisms.

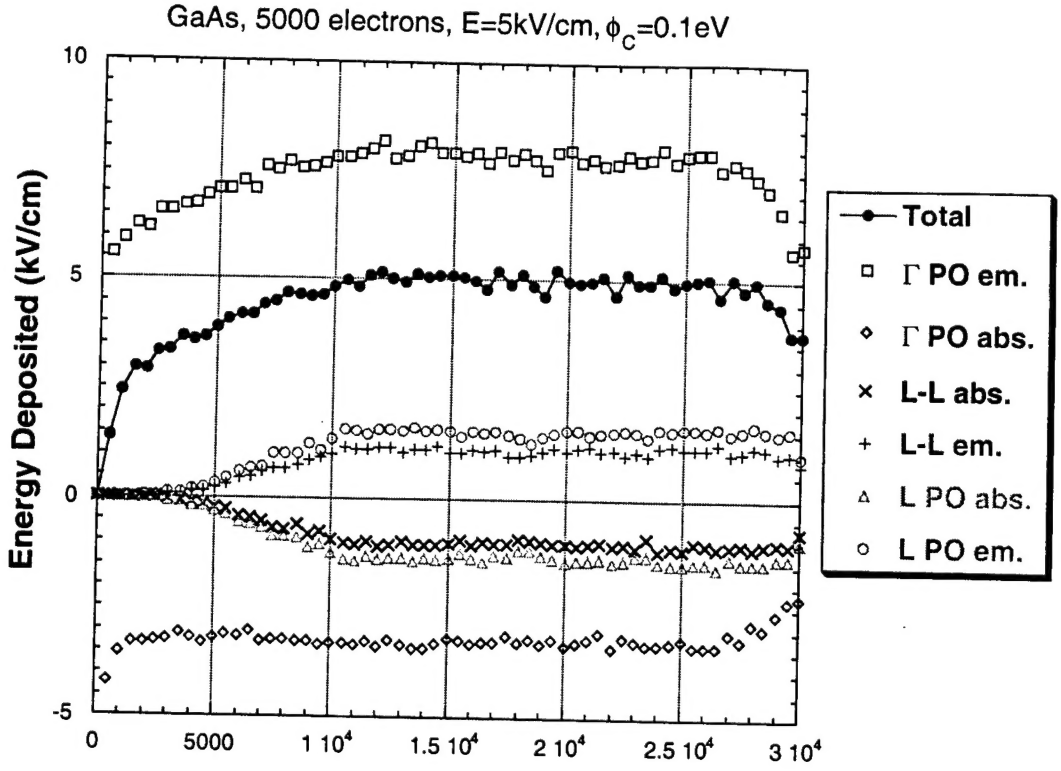


Fig. 1 Monte Carlo simulation of Joule heating as a function of distance for 5000 electrons injected over a 0.1 eV barrier into a 3-micron thick GaAs layer. Various curves show different energy loss mechanisms in a thin barrier heterostructure device. The important processes are Γ-valley polar optical phonon (PO) emission and absorption, L-valley PO phonon scattering and inter L-valley scattering (L-L).

Using various material parameters of InGaAs, and taking 0.4 μm for energy relaxation length, we can calculate the net cooling power at the cold side as a function of the thickness of the barrier for different cathode barrier heights (Fig. 3). The anode barrier height does not enter directly in the calculation of maximum cooling power. It is assumed to be high enough to suppress the reverse current form the hot to the cold side. It can be seen that at room temperature, thermionic cooling can maintain a temperature gradient of 10 degrees over a distance of 2 microns and provide a net cooling power of couple of 100 W/cm^2. The currents required for this cooling are on the order of 50 kA/cm^2.

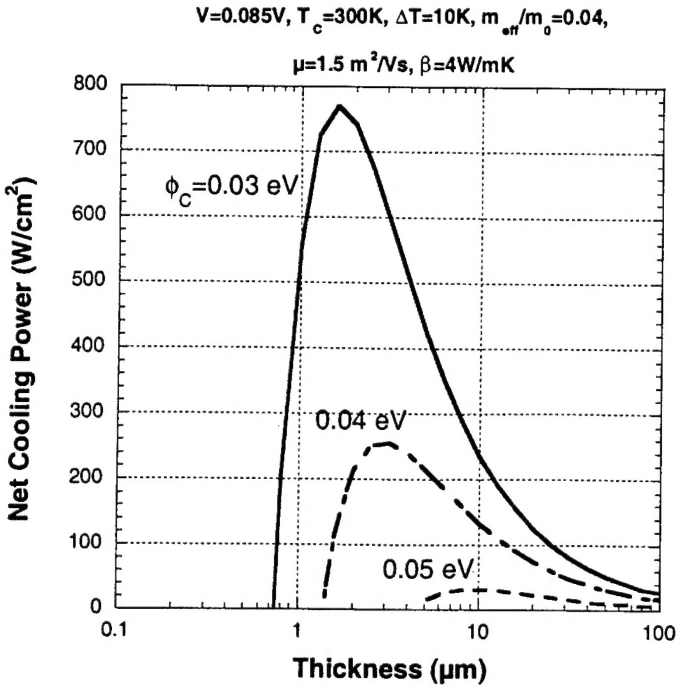


Fig. 3 Theoretical net cooling power density for InGaAs barrier as a function of barrier thickness.

Experimental results

In order to investigate experimentally thermionic emission cooling in heterostructures, a single InGaAsP (λ_{gap}=1.3 μm) barrier surrounded by n^+ InGaAs cathode and anode layers was grown using metal organic vapor phase epitaxy (MOCVD). Cathode and anode layer thicknesses were 0.3 and 0.5 μm and they were doped to $3x10^{18}$ cm^{-3}. The barrier layer had an n-doping of $2x10^{17}$ cm^{-3} and was one micron thick. Mesas with an area of 90x180 μm^2 were etched down using dry etching techniques. Ni/AuGe/Ni/Au was used for top and bottom contact metallization. Fig. 4a displays the temperature on top and on the bottom of the device as well as the substrate temperature far away from the device as a function of current. All temperatures are relative to the value at zero current. The rise in substrate temperature is an indication of the relatively high thermal resistance of ceramic package and the soldering layer used to mount the sample. Despite the poor performance of the heat sink on the anode side, a net cooling of 0.5°C is observed on top of the device. This cooling over 1 μm thick barrier corresponds to cooling capacities on the order of 200-300 W/cm^2. To understand these results a two dimensional finite difference heat equation solver (ANSYS) was used to simulate the performance of the device. Joule heating in the layers, substrate, and gold wire bonds were included as well as thermionic emission cooling (heating) at the cathode (anode) junction and the thermoelectric effect at the metal/semiconductor junctions. The Peltier effect at the junction InGaAs(n^+)/Au was studied by applying current between two bottom contacts. A cooling 2-3 times smaller than the thermionic cooling was measured.

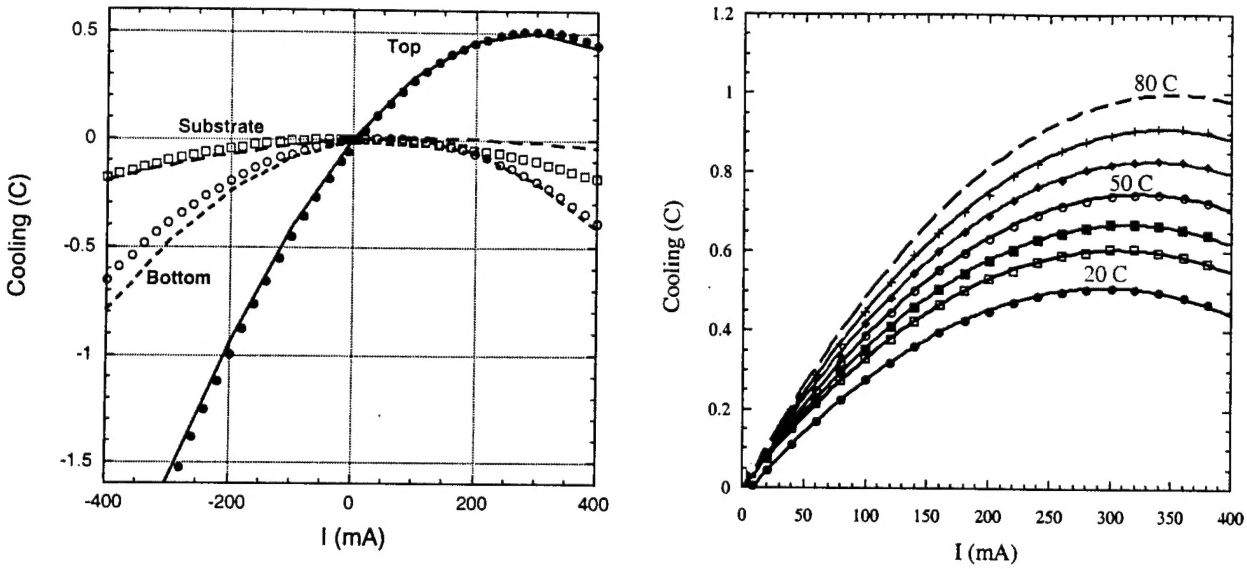


Fig. 4 (a) Measured temperature on top and on the bottom of the HIT cooler, as well as the substrate temperature far away form the device as a function of current. All temperatures are relative to the value at zero current. The heat sink temperature is 20°C. The simulation results are solid curve for top temperature, short-dashed curve for bottom temperature and dashed curve for the substrate. (b) Measured cooling at various substrate (heat sink) temperatures.

Assuming the thermal conductivity of InGaAsP to be 2 W/mK (i.e. 50% of textbook value [17]) and a solder layer and package with total thermal resistance of 2.5×10^3 K/W, the overall cooling and the temperature distribution in the device fit reasonably well the measured values in Fig. 4a. The simulation results are solid curve for top temperature, short-dashed curve for bottom temperature and dashed curve for the substrate. In order to minimize the effect of series and contact resistances, a number of p- and n-type HIT coolers connected electrically in series and thermally in parallel should be used (similar to conventional thermoelectric cooling modules). By improving the packaging, 10°C cooling for single stage InGaAsP HIT coolers is expected.

Fig. 4b displays the measured cooling at various substrate temperatures. The device cools much better at higher temperatures. A net cooling of about 1°C is measured at 80°C. The reason for the improved performance is two fold. First, the thermal conductivity of the barrier decreases at higher temperatures, and second, thermionic emission cooling increases due to the larger thermal spread of carriers near the Fermi energy.

The above theoretical and experimental results indicate the potential of HIT devices to achieve high cooling power densities. These devices have, however, a low efficiency (a

few % of the Carnot value). The main problem is that the high cooling power at the cathode should fight the large heat flux that is coming from the hot junction only 1 or 2 μm away. As it can be seen in Fig. 3, the device cannot achieve net cooling when the barrier is thick. For the case of thick barriers, electron transport is not any more determined by the "supply" of electrons at the cathode. One thus loses the advantages of thermionic emission cooling.

Smaller size coolers demonstrated the largest absolute cooling. Since a smaller device requires less current to achieve the same temperature gradient, there is less current for parasitic Joule heating from the wire bonds and contact resistance, and the overall cooling is larger. Increasing the heat sink temperature also resulted in a further increase in cooling. Figure 5 shows the maximum cooling increasing from 1.15°C to 2.25°C when the heat sink temperature was raised from 20°C to 90°C. One reason for the improvement is the larger thermal spread of carriers at higher heat sink temperatures that allows for more carriers to pass over the heterojunction barrier. The other reason is the reduced thermal conductivity of the barrier material cutting the amount of heat that returns to the cold junction.

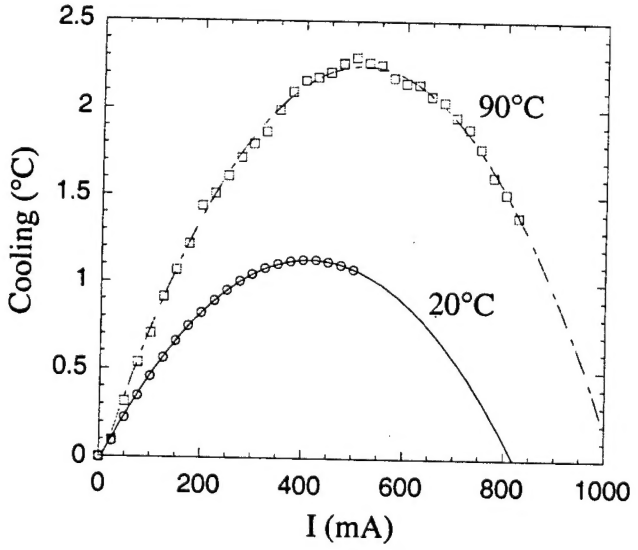


Fig. 5 Measured cooling at heat sink temperatures of 20 °C and 90 °C.

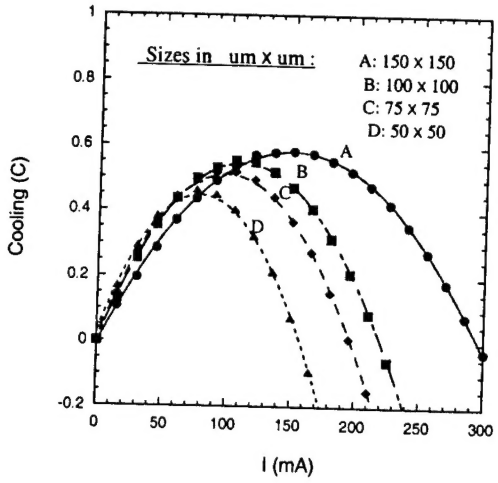
Experimental results for p-InGaAsP superlattice structures

A single InGaAsP superlattice barrier surrounded by p^+-InGaAs cathode and anode layers was grown using metal organic chemical vapor deposition (MOCVD). Cathode and anode layer thicknesses were 0.3 and 0.5 μm and the whole structure was doped to $1x10^{19}$ cm^{-3}. Mesas ranging in area from 20x20 up to 150x150 μm^2 were etched down using dry etching techniques. Ni/AuGe/Ni/Au was used for top and bottom contact metallization. The barrier itself consists of 1 micron thick superlattice (each period is 10nm InGaAs/ 5nm InGaAsP barrier with $\lambda_{gap} = 1.3\mu m$). In conventional multi-element TE-coolers, cascading of alternate p and n elements provides a way to send current to an array of coolers electrically in series and thermally in parallel. This will keep the cooling region far from the joule heating of the wires and reduces the effect of contact resistance by changing the trade off between current and voltage necessary to cool a given surface. However, in a single stage HIT cooler, one has to find a way to send the current to the cold junction on top of the device. This may be done simply by using a wire bonded to the top contact, but this heats up the device and significantly reduces the cooling power density. An alternate way would be through a side contact with a metal strip connecting the wirebond to the top of the device. This keeps the wirebond heat far from the device. This metal strip should be electrically isolated from the substrate, so a layer of Silicon-Nitride is deposited underneath. Experimental results and data analysis of initial devices showed that this layer bypasses the wirebond heating quite well to the heat-sink, but provides a way to transfer the substrate heat to top contact as well.

Temperature measurements are performed for different size coolers at several stage temperatures. A micro-thermocouple with 25um wire and 50 um tip diameter was used to measure the temperature on top of the device. The device is on a temperature-controlled stage and current is injected through the top contact into the device.

Figures 6 shows the experimental cooling results the temperature difference between the top contact and the heat- sink, vs. applied current. Figure 7 shows the simulations. There are various parameters that make the measured data to deviate from ideal behavior. For example the thermocouple on the top contact is a heat load connected to ambient temperature and makes the cooling results substantially worse for smaller devices

Theoretical modeling predicts that by reducing ohmic contact resistance down to $0.5*10^{-6}$ Ω-cm^2 and by eliminating side-conduction and substrate joule heating, the device can ultimately cool down by over 15 degree which corresponds to cooling power densities of over kW/cm^2. Figure 8 shows the predicted curves. Thermocouple effect is excluded in the calculations here.



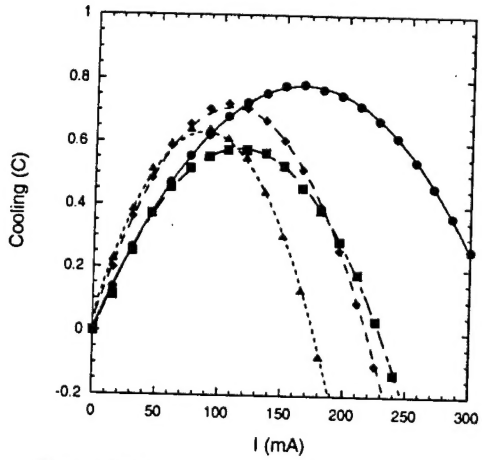
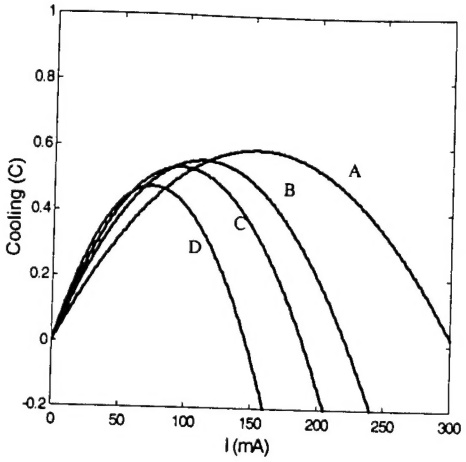


Figure 6:Measurements results for cooling of different size devices at (a) room temperature (b) 70C.



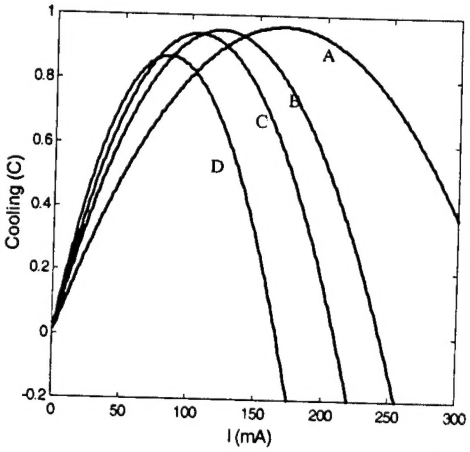
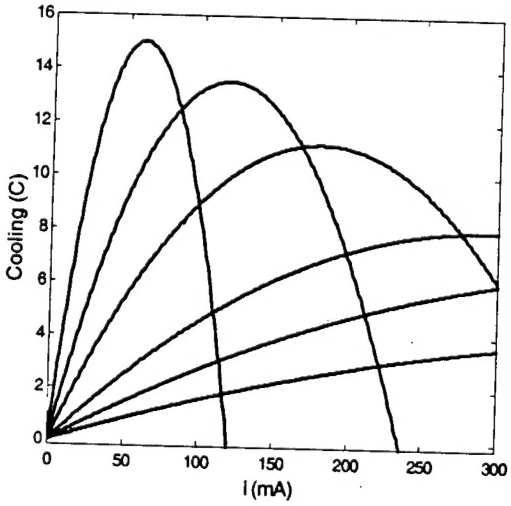


Figure 7:Simulation results for cooling of different size devices at (a) room temperature (b) 70C.



Sizes in um x um : A: 150 x 150
B: 100 x 100
C: 75 x 75
D: 50 x 50
E: 35 x 35
F: 20 x 20

Figure 8. Predicted cooling-current curves for different device sizes at room temperature.

Low Temperature Cooling Results:

Traditional thermoelectric coolers do not perform well at low temperatures. No solid state cooler can achieve liquid nitrogen temperatures down from room temperature. Using thermionic emission in heterostructures one can optimize the barrier height for selective emission of hot electrons for different ambient temperatures. Fig. 9 shows the preliminary experimental results for 2 micron thick InGaAs/InP superlattice structures. This structure was grown using MOCVD and it consisted of 80 period superlattice (20nm InGaAs and 5nm InP layers) doped to 6.5×10^{18} cm^{-3}. The measurements were performed at different ambient temperatures 100-300K using custom modified thermocouple probes in a cryostat. For the above structure the cooling is reduced by a factor of 20 at low temperatures. This is due to the fact that the superlattice barrier is designed for room temperature operation, i.e. the barrier is within 25meV of the Fermi energy in the material. In order to improve the low temperature performance, one has to design multiple stage cooler with optimize barrier height and doping profile in each stage.

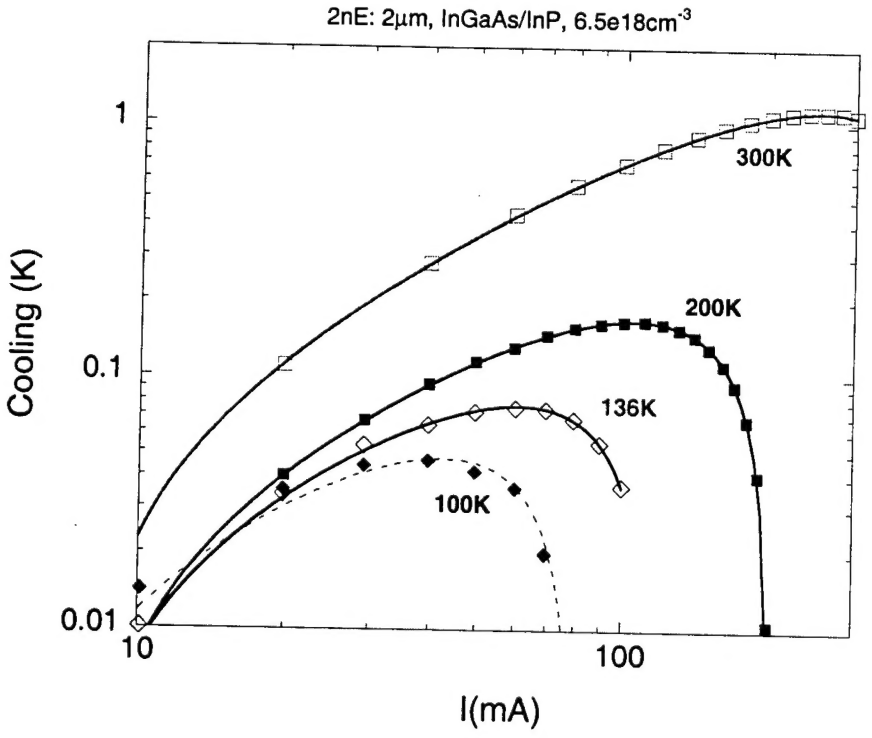


Figure 9. Experimental cooling for 2 micron thick InGaAs/InP superlattice structure at different ambient temperatures 100-300K.

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